

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Saket Goyal
Santhanakris Raman
Prabhakaran Krishnamurthy
Prasad Subbarao
Manjunatha Gowda

Serial No. : 09/997,888

Filed : November 29, 2001

For : Distributed Delay Prediction Of
Multi-Million Gate Deep Sub-
Micron ASIC Design-

Group Art Unit : 2123

Examiner : Thangavelu, Kandasamy

Atty Docket : / 01-536

I hereby certify that this correspondence is being deposited with the U.S.
Postal Service as First Class Mail in an envelope addressed to: Commissioner
for Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on the date below:

Manu Kashyap

12/14/05
Date

Signature

SUBMISSION OF FORMAL DRAWINGS PURSUANT TO 37 C.F.R. §1.85

Official Draftsman

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicant hereby substitutes the enclosed formal drawings for those presently in the above referenced application.

LSI Logic Corporation
1621 Barber Lane, MS D-106
Milipitas, CA 95035
408-433-7475

Date: 13 Dec 05

Respectfully submitted,



Timothy Croll

Reg. No. 36,771